Microwave Integrated CMOS Oscillators on Silicon-on-Insulator Substrate

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Abstract **- This paper shows the feasibility of implementing CMOS microwave oscillators on Silicon-on-Insulator (SOI) substrate at 5.8 and 12 GHz. The oscillators have been designed by introducing in a circuit simulator (SPICE) the SOI MOSFET's models developed at our laboratory. The models and the fabrication process of 0.25 µm channel length Fully Depleted (FD) SOI MOSFET's were not yet optimized for the first oscillator designs presented in this paper. However, the results show the potentiality of SOI CMOS technology for building low-power, low-voltage RF circuits.**

I. INTRODUCTION

The wireless market growth leads to an increasing interest in integrating RF receivers on silicon technologies. Thin film FD SOI CMOS technology is a very attractive candidate for low-power, low-cost microwave circuits, because of its excellent performances in terms of gain, speed and cut-off frequency [1]. Current gain cut-off frequency (f_T) and a maximum oscillation frequency (f_{max}) of 25 GHz and 70 GHz, respectively, have been measured at 1 V for 0.25 µm salicided FD SOI nMOSFET's LETI technology. An accurate microwave characterisation of the MOS transistors has led to the development of a non-linear high frequency model. This model has been used for designing oscillators at 5.8 GHz (the WLAN frequency) and 12 GHz.

II. MICROWAVE CHARACTERISTICS OF FD SOI MOSFET

An accurate on-wafer characterization technique has been developed at our laboratory [2], in order to evaluate the transition frequencies of the current gain (H_{21}) and the unilateral gain (*MA/SG*), as well as to extract the small signal equivalent circuit of the transistors. Fig. 1 represents the evolution of those measured cut-off frequencies versus bias conditions for a salicided and a non-salicided FD SOI MOSFET's composed of 12 parallel connected gate fingers of 0.25 µm channel length and 6.6 µm gate width, noted 12*(6.6/0.25). Due to the good microwave performances of FD SOI MOS transistors, there was a need for an accurate submicron RF model with adequate non quasi-static extensions, which could be introduced in usual simulators. The existing models, such as BSIM3v3, were not adequate for high frequency design [3]. The model developed here is based on a complete extrinsic small-signal equivalent circuit, dealing with the complex behavior of the lossy SOI substrate and a non-linear charge-sheet model for the intrinsic device [4]. The intrinsic model takes into account the channel length propagation delay by dividing the transistor channel into a series of shorter transistors. The model has been validated for frequencies up to 40 GHz and effective channel lengths down to 0.16 µm [5]. The main transistors parameters used for the oscillator design are given in Table 1.

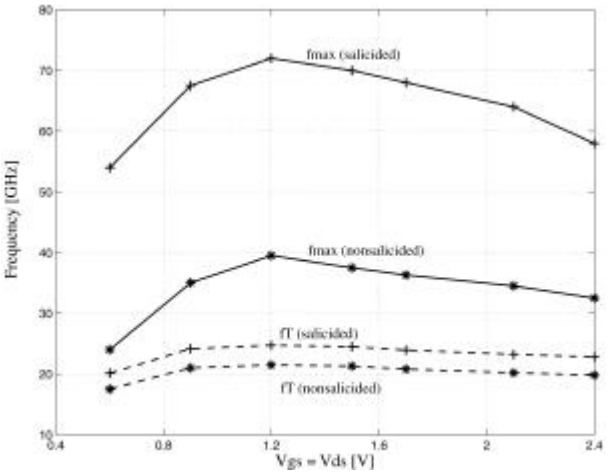

Fig. 1. Transition frequencies f_T (--) and f_{max} (-) for non-salicided (*) and salicided (+) 12*(6.6/0.25) FD SOI n-MOS transistors.

Extrinsic parameters	R_{ge} [Ω]	R_{de} [Ω]	R_{se} [Ω]	L_{ge} [pH]	L_{de} [pH]	
	155	5.4	5.1	32	30	
	$C_{gse} = C_{gde}$ [fF]			C_{dse} [fF]		
	21			12.8		
Intrinsic parameters	G_m [mS]	G_d [mS]	C_{gsi} [fF]	C_{gdi} [fF]	R_{gsi} [Ω]	*Delay* [ps]
	36.1	2.8	70.2	2.4	2.5	0.35

Table 1. Extracted small-signal parameters values for a non-salicided 12x(6.6/0.25) FD SOI MOSFET at V_{ds} = V_{gs} = 1 V.

III. OSCILLATOR DESIGN

Two basic oscillator families are used in the microwave frequency domain: series and parallel feedback oscillators [6]. Their schemes are represented in Fig. 2. Due to high substrate losses and source biasing difficulties, parallel feedback structures have been preferred to series feedback ones. We designed one with active feedback and a second one with passive feedback (inductance). The active feedback structure is represented in Fig. 3. It can be considered as 2 inverters face to face, with an inductance tank in parallel. The oscillation criterion imposes that the impedance of the inductance Z_L should meet the following conditions [7]:

$$Re(Z_L + Z_{out}) < 0$$
$$Im(Z_L + Z_{out}) = 0$$

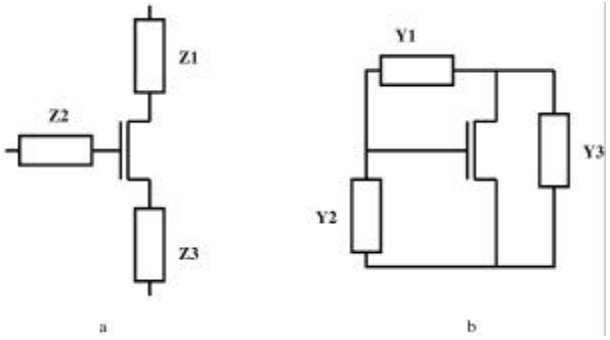

Fig. 2. Microwave oscillators structures (a) series feedback, (b) parallel feedback.

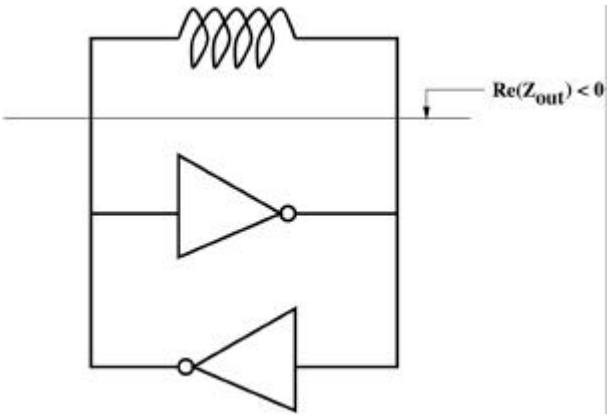

Fig. 3. Active feedback oscillator structure.

At 5.8 GHz, for a FD SOI n-MOSFET with dimensions 12x(6.6/0.25) biased in weak inversion, the impedance seen at the inverters input is Z_{out} = -70.6-j96.3 Ω. This value is deduced from measurements and simulations on existing devices using models developed at the laboratory. So, the needed inductance should have the following characteristics: $L \approx 2.5$ nH and $Q_L > 4$. These performances can be easily achieved on SOI substrate with a spiral inductor [8]. The inductive feedback circuit structure is typically the one presented in Fig. 2b. Expressions for the different admittances can be found in the literature. Those given in [6] allow to reach a good trade-off between circuit instability and output power. The computed circuit elements from [6] are the following values: L_1 = 4 nH, C_2 = 0.1 pF, C_3 = 0.18 pF. To reduce circuit size, the capacitor C_3 will be distributed between a parallel metallic plates capacitor and the input capacitor of the output buffer. However, in order to keep a good quality factor of the total equivalent capacitor – which is altered by the MOS gate resistance – the input transistor will be designed with a large number of parallel connected short gate fingers. The circuit schematic is presented in Fig. 4.

IV. CIRCUIT FABRICATION

The circuits were fabricated on a standard SOI substrate with a resistivity of about 20 Ω.cm. The transistors are FD SOI MOSFET's with a channel length of 0.25 µm for the active feedback oscillator and 0.35 µm for the inductive feedback oscillator. Capacitors were fabricated using MIM structures which give the best quality factor for the values needed. Inductors has been realised with square spiral structures using two metal layers. With such a structure, an inductor with a value of 4 nH and a quality factor of 8 can be achieved up to 10 GHz.

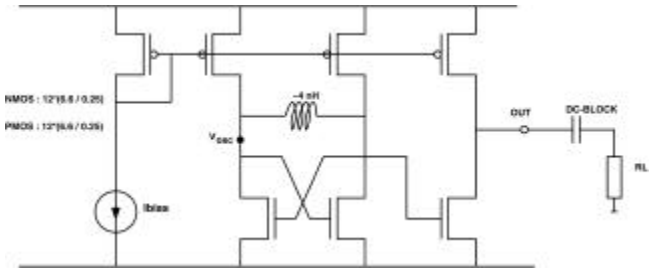

Fig. 4. Active feedback oscillator circuit.

V. MEASUREMENTS AND DISCUSSIONS

Circuits are measured on-wafer with coplanar probes having a pitch of 150 µm and a DC probe allowing on-wafer circuit biasing. The oscillator output is connected to a spectrum analyser having an input impedance of 50 Ω. A part of the measurements are presented in Fig. 5 (output power) and Fig. 6 (output power and oscillation frequency versus bias voltage).

The active feedback oscillator shows a maximum output power of – 19 dBm with a bias voltage of 1.4 V and a total current of 3.44 mA (and 1.36 mA for 1.2 V) for a total power consumption of 4.8 mW. So each transistor is driven by a drain-source current of about 900 µA. These results are comparable with those presented in [9-11]. However, it has to be kept in mind that the transistors were not optimized at the time the layout was

produced, mainly the p-MOS transistors, due to a fabrication problem in the previous process.

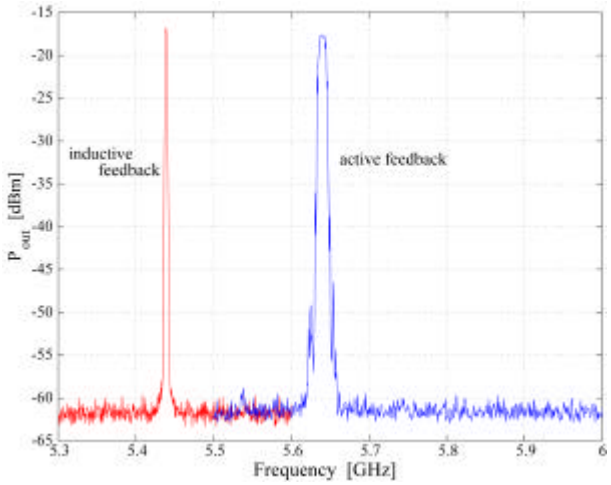

Fig. 5. Spectral behavior for passive and active parallel feedback oscillators.

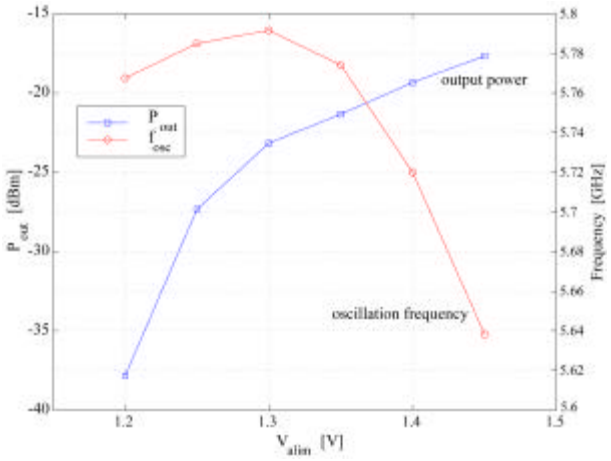

Fig. 6. Output RF power and oscillation frequency versus bias voltage for the active feedback oscillator using a spiral inductor of 4 nH.

The p-MOS transistors operated in saturation, instead of weak inversion as desired, so it should be possible to reduce again bias voltages probably near 1 V by optimizing their behavior. Moreover, it is important to note that power level measured by the spectrum analyzer is the output power coming from the oscillator diminished by the output buffer consumption. The output buffer is needed for "matching" condition purposes with the 50 Ω input of the spectrum analyzer. Of course, in a real transceiver chain of communication system that power loss will not appear.

Fig. 7 represents the peak-to-peak voltage at the oscillator output (noted V_{osc} in Fig. 4) for an oscillator design based on salicided and non-salicided 0.25 µm FD SOI MOSFET's versus frequency for a L tank at constant Q_L and with various inductance values depending on the desired oscillation frequency.

The simulations show clearly that the salicide process used for reducing the contact area resistances of the transistor allow to increase the working frequency of the designed oscillator for a given output power level or to rise the output power level for a fixed oscillation frequency.

Recent measurements have confirmed the conclutions of those simulations. Fig. 8 shows the RF output power and the oscillation frequency versus bias current for two active oscillators: the first one uses non-salicided 0.25 µm FD SOI MOSFET's and a L tank of 4 nH and the second one is based on salicided 0.25 µm FD SOI MOS transistors and a L tank of 1.2 nH. By reducing the indutance value of the L tank by a factor 3.33 and using the salicide process to reduce the transistor access resistances, we observed that the oscillation frequency is double for the active oscillators measured under the same bias conditions.

Fig. 9 presents the DC power consumption of non-salicided and salicided active oscillator designs versus bias current. Interesting microwave characteristics have been measured for all oscillator designs at low power consumption (below 10 mW). These first results render the FD SOI CMOS technology very attractive for low-power RF circuits.

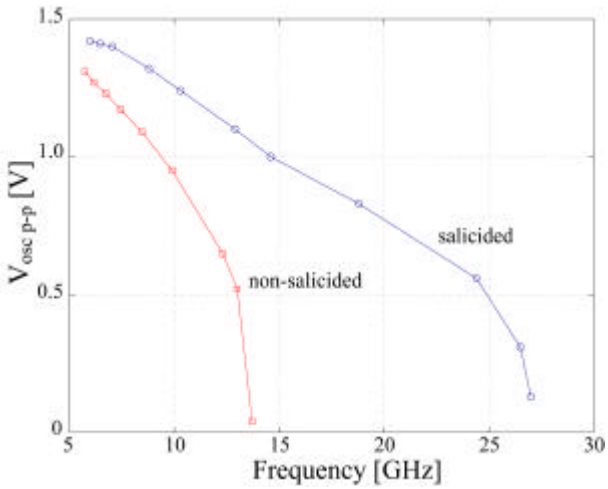

Fig. 7. Peak-to-peak voltage at the oscillator output versus the oscillation frequency for a salicided (○) and non-salicided (□) designs.

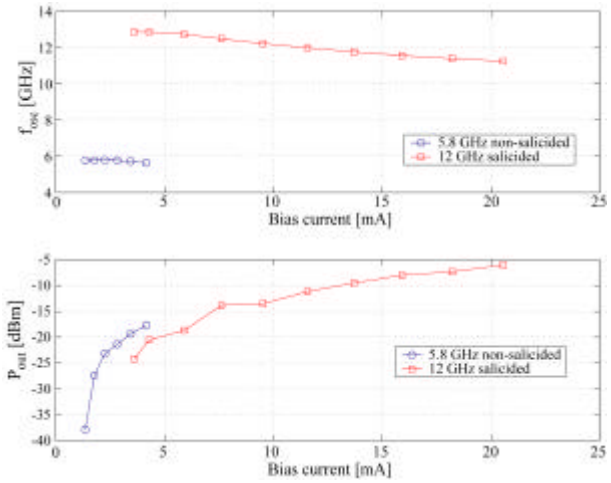

Fig. 8. Output RF power and oscillation frequency versus bias current for active feedback oscillator designs at 5.8 and 12 GHz.

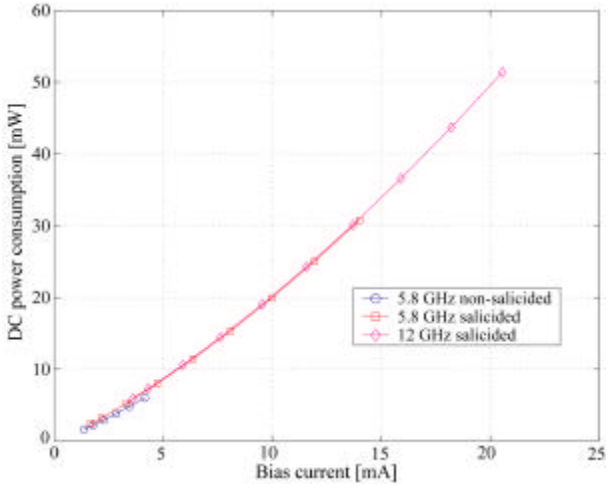

Fig. 9. DC power consumption for three different oscillators.

VI. CONCLUSIONS

Classical microwave oscillator structures has been successfully implemented on SOI substrate. The results obtained demonstrate the possibility to reduce effectively the number of devices used and the bias voltage less than 1 V which follows the current trend in circuit design for wireless communications. Further results could be obtained by optimising the MOSFET's performances such as the p-MOS behaviour in weak inversion as well as the gate resistance which is critical for the device transition frequency. This could lead to increase the oscillation frequency or decrease the bias voltage.

VII. ACKNOWLEDGEMENT

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